Claims:

4. (Currently Amended) In a method for operating a processor wherein a sequence of one or more instruction words are derived from a translation of program code, each instruction word having a plurality of instruction word parts, each word part arranged to trigger a functional unit of a processor, and wherein said instruction word parts are formed into program words and said program words are used to form secondary instruction words for operating said processor which are stored in a secondary instruction word memory; the improvement wherein the operation of the processor is divided in an execution phase and a preceding configuration phase, wherein ~~the~~ during ~~a~~ the preceding configuration phase instruction word parts corresponding to data-stationary commands are assembled as complex words in a complex word sequence, identified by a complex word pointer and stored in a complex word table at a location corresponding to said pointer, wherein said complex word pointers are provided as program words corresponding to said data-stationary commands, and wherein upon encountering said complex word pointers in said program words during ~~an~~ the subsequent execution phase, said complex words are read from said complex word table and stored in parallel in said secondary instruction word memory, whereby the use of translation buffers during execution is avoided.

5. (Previously Presented) A method as specified in claim 4 wherein said complex words further include assignments for storage of said complex words in said secondary instruction word memory.

6. (Previously Presented) A method as specified in claim 4 wherein said secondary instruction word memory is operated in a fixed sequence

7. (Currently Amended) In a processor wherein program codes are translated into a sequence of instruction words, each having a plurality of instruction word parts, each word part being arranged to trigger a functional unit of a processor, and wherein instruction words are sequentially provided to said processor functional units via a buffer memory, the improvement wherein the program codes are completely translated into the sequence of instruction words during a configuration phase for execution in a subsequent execution phase, wherein there is provided a memory for storing instruction word parts corresponding to data-stationary commands, said instruction word parts being stored during ~~a~~ the configuration phase at a location corresponding to a complex word pointer corresponding to a data-stationary command, and wherein said memory is arranged to directly transfer said complex word parts to said buffer memory in parallel to execute a data-stationary command during the subsequent execution phase.

8. (Previously Presented) The improved processor as specified in claim 7 further having an execution memory wherein instruction word sequences are stored in the form of program words, and wherein there is provided a configuration processor for storing said complex word pointers as program words in said execution memory for data-stationary commands.